REMARKS

Claims 1 to 20 are pending in this application. Claims 1, 10 and 16 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Applicants spoke with the Examiner's supervisor on Friday, June 27, 2008. Applicant's undersigned representative requested a telephonic interview with the Examiner and the Examiner's supervisor to discuss this Office Action response. The Examiner's supervisor agreed to have a meeting once this response was received by the Examiner. The Examiner is requested to call the Applicants' undersigned represenataive to set-up the teleconference.

Claims 1 to 9 were rejected under 35 U.S.C. § 112, second paragraph because it was allegedly not clear what "the data buffer" refers to. Based on the foregoing claim amendment, Applicants respectfully request withdrawal of the §112 rejection.

Claims 1, 4 to 7, 9 to 11 and 13 to 19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Gaddis et al. (U.S. Patent Number 5,815,501 hereinafter "Gaddis"). Claims 2 and 22 were rejected under 35 U.S.C. § 103(a) as being obvious over Gaddis in view of Vogel (U.S. Patent Number 6,075,788 hereinafter "Vogel").

Claim 1 is directed to an ATM-Ethernet network system includes an ATM processor, an Ethernet network processor and an ATM-Ethernet processor interfacing between the ATM processor and the Ethernet network processor. The ATM-Ethernet processor includes a packet buffer pointer ring for managing traffic from the Ethernet network processor to the ATM processor. The packet buffer pointer ring contains a plurality of ATM processor packet buffer

pointers each including a memory address in a packet buffer of the ATM processor. The ATM-Ethernet processor also includes a packet descriptor ring and a data buffer for managing traffic from the ATM processor to the Ethernet network processor. The packet descriptor ring being configured to contain a plurality of packet descriptors each including an ATM-Ethernet packet buffer memory address in the data buffer.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1. In particular, Gaddis does not disclose or suggest an ATM-Ethernet processor includes a packet buffer pointer ring for managing traffic from the Ethernet network processor to the ATM processor.

The Examiner has not shown in Gaddis what he is equating as a packet buffer pointer ring. The Examiner never specifically identifies what in Gaddis he is equating to a packet buffer pointer ring. The Examiner has equated the control microprocessor to the ATM-Ethernet processor (see page 3 of the Office Action). However, Gaddis does not teach that the control microprocessor includes a packet buffer pointer ring much less a packet buffer pointer ring for managing traffic from the Ethernet network processor to the ATM processor.

Since the packet buffer pointer ring is a structure, the Examiner must identify explicitly the recited structure in Gaddis. If the Examiner is indicating that it is inherent then Applicants respectfully request that the Examiner provide support (See MPEP §2112 Section IV). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic (see In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); In re Oelrich, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981)). "To establish inherency, the extrinsic evidence 'must make clear that the missing

descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient' " (emphasis added, see In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)).

Also, Gaddis does not disclose or suggest a packet buffer pointer ring that contains a plurality of ATM processor packet buffer pointers each including a memory address in a packet buffer of the ATM processor. The Examiner has indicated that "it is believed the portal includes memory address pointing to specific port/destination/queue in the ATM network" (emphasis added, see page 9 of the Office Action). Applicants respectfully submit that what the Examiner's believes is not a basis for a §102 rejection. The cited art in a §102 must explicitly show each and every claim element. If the Examiner intends that this rejection be a §103 instead, he should change the rejection.

Since the Examiner has failed to show each and every claim element, the Examiner has not established a *prima facie* anticipation rejection.

Claim 10 has corresponding features to claim 1. Applicants submit that the cited references should also be withdrawn with respect to claim 10 for at least the same reasons as claim 1.

With respect to claim 16, Gaddis does not disclose or suggest analyzing the packet descriptor for error and if error is detected dropping the packet descriptor and reporting error to the ATM processor. Applicants note that the Examiner has cited huge portions of Gaddis, but none of the portions of Gaddis disclose or suggest analyzing the packet descriptor for error and if

error is detected dropping the packet descriptor and reporting error to the ATM processor. The Examiner has not even identified in Gaddis what he is equating as a "packet descriptor." Again, the Examiner has failed to make a *prima facie* rejection because the Examiner has not explicitly shown all of the claim elements.

For at least the foregoing reasons, Applicants request withdrawal of the art rejection.

Applicants submit that all dependent claims now depend on allowable independent claims.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for withdrawing the prior art cited with regards to any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

It is submitted that this amendment places the application in condition for allowance or in better form for consideration on appeal, and thus, entry of this amendment is respectfully requested under the provisions of 37 C.F.R. §1.116.

Applicants' attorney can be reached by telephone at (781) 401-9988 ext. 123.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 50-0845 referencing Attorney Docket: INTEL-048PUS.

Respectfully submitted,

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